omitted from the table. Also, the following text was added to the specification because it was in the table of Appendix A but accidently omitted from the specification:

> Next, the photoresist is removed and a new layer of photoresist is deposited and developed using mask 12 to protect the EEPROM device and the N well 62 of the PMOS device area and expose the P well 66 of the NMOS device. An N+ arsenic implant is performed using this layer of photoresist and the control gate 110 and oxide spacer layers 114 of the NMOS device as implant masks to form self aligned source and drain layers 130 and 132 for the NMOS device.

IN THE CLAIMS

1. (CLEAN) A nonvolatile memory cell comprising:

a semiconductor substrate doped to have a first conductivity type so as to act as a source region of said nonvolatile memory cell, said first conductivity type being either N-type or P-type, and having a top surface which extends laterally and a depth which extends vertically;

a vertical MOS transistor formed by alternating, abutting N-type and P-type doped layers in said substrate which have junctions therebetween to form a channel region and a drain region of said vertical MOS transistor with said drain region having said first conductivity type and said channel region having a second conductivity type which is P-type if said first conductivity type is N-type and is N-type if said first conductivity type is P-type, said substrate forming a source region of said first conductivity type of said vertical MOS transistor, said source regions having a junction with said channel region, and wherein a well with one or more walls is etched vertically into said substrate through said channel and drain regions and at least partially into said source region such that said drain and channel regions surround said well and form at least a portion of said

one or more walls of said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well, said edges being defined by said one or more walls of said well, and insulated from said channel and drain regions and said substrate by a layer of insulating material, said floating gate being laterally adjacent to at least said portion of said wall of said well formed by said channel region of said vertical MOS transistor such that differing levels of trapped charge in said floating gate affects the conductivity of said channel region and a threshold of said vertical MOS transistor;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend vertically down into said well and lie laterally adjacent to said floating gate but be insulated therefrom by an insulation layer such that voltage applied to said control gate affects the charge on said floating gate; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with said drain region of said vertical MOS transistor.

2. (CLEAN) A substructure of a vertical MOS transistor forming part of a nonvolatile memory cell comprising:

a semiconductor substrate having a top surface which extends in a lateral direction and a thickness which extends in a vertical direction and having a drain region of a first conductivity type formed therein and suitable to act as a drain of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a

vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type and suitable to act as a source of a vertical MOS transistor;

a well etched vertically into said semiconductor substrate, said well having one or more side walls and being deep enough to penetrate through said drain region, said channel region and at least partially into said source region such that at least some portions of said one or more side walls of said well are defined by intersections with said source, drain and channel regions;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on said one or more sidewalls of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond said one or more of said well and positioned laterally adjacent to the intersection of said one or more side walls and said channel region such that trapped charge in said floating gate affect the conductivity of said channel regions and a threshold of said vertical MOS transistor;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures; and

a word line comprising conductive material deposited so as to extend into said well far enough to lie laterally adjacent to said floating gate so as to form a control gate of a vertical MOS transistor nonvolatile EEPROM structure.

3. (CLEAN) A nonvolatile memory cell comprising:

a semiconductor substrate having a top surface which extends laterally and having a depth which extends vertically;

a vertical MOS transistor formed by a first layer of said substrate of N-type conductivity forming a drain region of said vertical MOS transistor, a second layer of said substrate of P-type conductivity and vertically adjacent to and beneath said first layer relative to said top surface of said substrate so as to form a channel region of said vertical MOS transistor, and a third layer of said substrate of N-type conductivity within said substrate and vertically adjacent to and beneath said second layer relative to said top surface of said substrate so as to form a source region of said vertical MOS transistor, said substrate also having a well vertically etched therein so as to penetrate through said first and second layers and at least partially through said third layer, said well having at least a portion of the wall or walls thereof formed by the intersection of said well with said channel regions, and said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond the wall or walls of said well, said floating gate including at least a portion thereof which lies laterally adjacent to said portion of said wall or walls of said well formed by the intersection of said well with said channel region such that trapped charge in said floating gate affects the conductivity of said channel regions and a threshold of said vertical MOS transistor, said floating gate being insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed so as to extend down into said well and have at least a portion thereof which is laterally adjacent to said floating gate but insulated therefrom by an insulation layer so as to act as a control gate for said vertical MOS transistor;

a bit line comprising a layer of conductive material formed above said top surface of said substrate so as to be in electrical contact with a portion of said first layer; and

a spacer layer of insulating material insulating said word line from said bit line.

4. (CLEAN) The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line is formed above said first layer so as to be above the top surface of said substrate and contacts said first layer at all points that form a top surface of said first layer between spacer layers of insulating material that insulates the word lines of adjacent memory cells.

Please add a new claim 7 as follows:

7. A vertically integrated nonvolatile memory transistor comprising:

a substrate having a top surface that extends horizontally and a depth which extends vertically and which is doped to a have a first conductivity type and having an active area therein doped to a second conductivity type and a conductivity level suitable to act as a source region of a vertically integrated MOS non volatile memory transistor;

a buried channel region in said active area doped to have said first conductivity type and a conductivity suitable to act as a channel region of said vertically integrated MOS non volatile memory transistor;

a drain region in said active area doped to have said second conductivity type and a conductivity suitable to act as a drain region of said vertically integrated MOS non volatile memory transistor;

a well etched vertically down through said drain and channel regions and at least partially into said source region;

an gate insulation layer formed on the walls of said well and an insulating layer on a floor of said well;

a conductive floating gate formed on the walls of said well on said gate insulation layer such that all portions of the walls of said well that intersect said channel region are horizontally adjacent said floating gate such that trapped charge on said floating gate can alter the conductivity of said channel region and the threshold of said vertically integrated MOS non volatile memory transistor;

an intergate insulation layer formed on said floating gate suitable to insulate said floating gate from all surrounding conductive structures;

a conductive control gate formed in said well so as to be horizontally adjacent to said floating gate such that a first potential applied to said control gate causes charges to tunnel into said floating gate and a second potential applied to said control gate causes charges to tunnel out of said floating gate, said control gate extending up to and making contact with or being part of a conductive word line formed across said top surface of said substrate;

a control gate insulating layer which insulates the top of said word line and one or more spacer insulation layers which insulate the sides of said word line;

one or more contact windows which are etched so as to be self aligned to the edge of said spacer insulation layers and which open said drain region to electrical contact; and

a conductive bit line formed across said top surface of said substrate so as to make contact with said drain region through said one or more contact windows.

Please add the following new claims.

8. The apparatus of claim 1 wherein said N-type and P-typed doped layers in said substrate forming said channel region and said drain regions are formed without

using any mask or only using non critical masks where non critical masks are defined as masks which are used to do only very loose alignment between layers.

9. The apparatus of claim 1 wherein said nonvolatile memory cell is formed with a process which simultaneously forms PMOS and NMOS devices on the same substrate as said nonvolatile memory cell but forms said PMOS and NMOS devices in different active areas from an active area in which said nonvolatile memory cell is formed, and wherein said source, channel and drain regions of said non volatile memory cell are formed with said process which simultaneously forms said PMOS and NMOS devices and are formed while said active areas of said PMOS and NMOS devices are covered by an insulation layer.

10. In a vertically integrated nonvolatile memory cell structure formed using a vertical well that penetrates doped drain and channel regions and into a source region of a substrate, said vertical well having a top edge and a bottom, said self aligned floating gate substructure comprising:

a self aligned floating gate insulating material layer on the vertical walls of said well which does not extend above said top edge of said well;

an insulating layer on said bottom of said well;

a self aligned floating gate conductor material formed on the layer of self aligned floating gate insulating material so as to not extend above said top edge of said vertical well.

11. The apparatus of claim 10 further comprising a self aligned layer of silicon dioxide/nitride/silicon dioxide (hereafter ONO) covering said self aligned floating gate

conductor material, and a doped polysilicon conductor control gate covering said ONO layer, said control gate being self aligned to an edge of said floating gate at said bottom of said well but extending above said top edge of said well, and a layer of silicon dioxide insulator covering a top surface of said control gate and self aligned spacer layers of silicon dioxide insulating vertical side edges of said control gate, said ONO layer being self aligned so as to not extend horizontally beyond the edges of said spacer layers of silicon dioxide insulator and insulating said control gate from said floating gate.

12. The apparatus of claim 11 wherein said self aligned floating gate insulating material layer, said insulating layer on said bottom of said well, said self aligned floating gate conductor material, said self aligned control gate and said self aligned ONO layer all are formed without using a critical mask, where a critical mask is defined as a mask which is required for tight tolerance alignment between different layers of a semiconductor structure.

product by process

13 . The apparatus of claim 10 wherein said self aligned floating gate substructure is formed by the following process:

forming a vertical well by etching vertically through a layer of silicon dioxide (herafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

anisotropically etching said nitride back from all horizontal surfaces to

leave nitride only on said vertical walls of said well;

growing a layer of oxide on said bottom of said well;

wet etching said nitride off said vertical walls of said well to expose said pad oxide;

growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

depositing a layer of doped polysilicon over said substrate and into said well to cover said vertical walls and bottom of said well;

forming a self aligned floating gate without using a mask by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and said bottom of said vertical well.

14. The apparatus of claim 11 wherein said self aligned floating gate substructure, said self aligned control gate and said self aligned ONO layer are formed by the following process: P by P

1) forming a vertical well by etching vertically through a layer of silicon dioxide (herafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

2) depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

3) anisotropically etching said nitride back from all horizontal surfaces to leave nitride only on said vertical walls of said well;

4) growing a layer of oxide on said bottom of said well;

5) wet etching said nitride off said vertical walls of said well to expose said pad oxide;

6) growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

7) depositing a layer of doped polysilicon conductor over said substrate and into said well to cover said vertical walls and bottom of said well;

8) forming a self aligned floating gate without using a mask by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and said bottom of said vertical well;

9) forming a layer of silicon dioxide insulator covered by a layer of nitride insulator covered by another layer of silicon dioxide insulator (hereafter ONO) over said oxide layer covering said top surface of said substrate, said ONO layer extending down into said vertical well and covering said self aligned floating gate;

10) depositing over said ONO layer a second layer of doped polysilicon conductor from which said self aligned control gate will be formed;

11) growing a layer of oxide over said second layer of doped polysilicon;

12) using a non critical mask to etch away portions of said second layer of doped polysilicon to define lateral extents of said self aligned control gate above said top surface of said substrate leaving said layer of oxide on a top

surface of said control gate;

13) depositing a layer of oxide over said surface of said substrate and covering said control gate's vertical side walls;

14) anisotropically etching back said layer of oxide deposited in step 13 to remove oxide only from horizontal surfaces and leaving spacer oxide only on vertical side walls of said polysilicon of said control gate;

15) using a non critical mask to define the lateral extents of contact holes to said drain region etching through said ONO layer formed in step 9 and said oxide layer covering said top surface of said substrate to self align said ONO layer to the lateral extents of said spacer oxide layer defined in step 14.

15. In a vertically integrated nonvolatile memory cell structure formed using a vertical well that penetrates doped drain and channel regions and into a source region of a substrate, said vertical well having a top edge and a bottom, a self aligned floating gate insulating layer substructure comprising:

fig. 5

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a self aligned floating gate insulating material layer on the vertical walls of said well which does not extend above the top of said well; and

an insulating layer on the bottom of said well.

16. The self aligned floating gate insulating material substructure of claim 15 manufactured by a process which does not use any critical mask in the steps used to form said self aligned floating gate insulating material layer such that it does not extend above said top of said well, where a critical mask is defined as a mask which is required for tight tolerance alignment between different layers of a semiconductor structure.